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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,533	02/27/2002	Hiroshi Hashimoto	020244	6400
38834 7590 10/26/2007 WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP 1250 CONNECTICUT AVENUE, NW SUITE 700 WASHINGTON, DC 20036				
EXAMINER				
LE, THAO X				
ART UNIT		PAPER NUMBER		
2814				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/083,533

Applicant(s)

HASHIMOTO ET AL.

Examiner

Thao X. Le

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 October 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4, 6-10 and 12-40 is/are pending in the application.
- 4a) Of the above claim(s) 16-39 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6-10, 12-15 and 40 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Attachment Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-646)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.
2. For the record, the Applicant's argument filed on 05 Oct. 2007 admitted that a bird's beak is formed in both EPROM and the peripheral transistors of Chang (US6004829).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

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4. Claims 1, 2-4, 7, 9-10, 12, 14, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6004829 to Chang (of record) et al in view of US 5506159 to Enomoto.

Regarding claims 1, Chang discloses a semiconductor integrated circuit (IC) device in fig. 4H, comprising: a substrate 110, a nonvolatile memory device T1 formed in a memory cell region of substrate 110 and having a multilayer gate electrode structure comprising a tunnel insulating film GX1 covering substrate 110 and floating gate electrode GC1 formed on the tunnel insulating film GX1 and having a side wall surfaces covered with a protection insulating film 15 formed of an oxide, col. 7 line 16; a semiconductor device T2 formed in a device region of substrate 110, the semiconductor device comprising a gate insulating film GX2 covering substrate 110 and gate electrode GC2, formed on the gate insulating film GX2; the gate insulating film GX2 is interposed between substrate 110 and the gate electrode GX2 have a thickness at the region under the entire gate electrode GX2, fig. 4H, wherein the bird's beak structure is formed at an interface of the tunnel insulating film GX1 and the floating gate electrode GC1 the bird's beak structure penetrating into the floating gate electrode GC1 along the interface from the sidewall faces of the floating gate electrode and sidewalls are formed over the protection insulating film 15, said side walls covering the entire surface of the multilayer gate electrode structure, fig. 4H, wherein the protective insulating film 15 continuously covers sidewall faces and a top surface of the multilayer gate electrode structure, fig. 4H; wherein the protective insulating film covers the multilayer gate electrode uniformly,

fig. 4H, and the multilayer gate electrode structure, including a control gate GC2 has a substantially uniform width, fig. 4H.

Note: The bird's beak structure as admitted by the applicant in the amendment dated 05 Oct. 2007.

But, Chang does not disclose the gate insulating film GX2 have a uniform thickness at the region under the entire gate electrode GC2.

However, Enomoto discloses a semiconductor device in fig. 10 comprising a memory, a tunnel oxide 5, a floating gate 6, a dielectric 7, a control gate 13, a peripheral transistor (with gate 12) comprising a gate insulating film 8 having a uniform thickness at the region under the entire gate electrode 12. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the gate insulating film having a uniform thickness at the region under the entire gate electrode teaching of Enomoto with Chang's device, because it would have exhibited better and more desirable characteristics such as reducing damage and contamination without incurring cost as taught by Enomoto in col. 1 lines 38-42 and col. 4 lines 28-37.

Regarding claims 2-3, 12, Chang discloses the IC device wherein the multilayer gate electrode structure further comprises an insulating film 120 formed on the floating gate electrode GC1, and a control gate electrode GC2 formed on the insulating film GC1, wherein each of the gate electrode GC2 and control gate electrode GC2 comprises doped polysilicon, col. 6 line 34.

Regarding claims 4 and 10, Chang discloses the IC device wherein the oxide film connects the bird's beak structure.

Regarding claims 7 and 14, Chang discloses the IC device having the tunnel oxide GX1.

Regarding claim 9, Chang discloses a semiconductor integrated circuit device in fig. 4H comprising: a substrate 110, a nonvolatile memory device formed in a memory cell region T1 of said substrate 110, the nonvolatile memory device comprising: a first active region S1 covered with a tunnel insulating film GC1, a second active region D1 formed next to the first active region S1 and covered with an insulating film 120, a control gate GC2 formed of an embedded diffusion region formed in the first active region; a first gate electrode GC1 extending on the tunnel insulating film GX1 in the first active region S1 and forming a bridge between the first and second active regions S1/D1 to be capacitive-coupled via the insulating film 120 to the embedded diffusion region in the first active region S1, the first gate electrode GC1 having sidewall faces thereof covered with a protection insulating film 15 formed of a oxide film; a diffusion region formed on each of sides of the first gate electrode GC1 in the first active region; and a semiconductor device formed in a device region T2 of substrate 110, the semiconductor device comprising a gate insulating film GX2 covering substrate 110 and a second gate electrode GC2 formed on the gate insulating film GX2, fig. 4H, wherein the bird's beak structure is formed at an interface of the tunnel insulating film and the floating gate electrode the bird's beak structure penetrating into the floating gate electrode along the interface from the sidewall faces of the floating gate electrode and

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sidewalls are formed over the protection insulating film, said side walls covering the entire surface of the multilayer gate electrode structure; wherein the protective insulating film 15 covers a top surface of the first gate electrode GC1 electrode uniformly; and the first gate electrode GC1 has a substantially uniform width, fig. 4H.

But, Chang does not disclose the gate insulating film is interposed between said substrate and the second the second gate electrode GC2 to have a uniform thickness at the region under the entire gate electrode GC2.

However, Enomoto discloses a semiconductor device in fig. 10 comprising a memory, a tunnel oxide 5, a floating gate 6, a dielectric 7, a control gate 13, a peripheral transistors (with gate 12) comprising a gate insulating film 8 having an uniform thickness at the region under the entire gate electrode 12. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the gate insulating film having an uniform thickness at the region under the entire gate electrode teaching of Enomoto with Chang's device, because it would have exhibited better and more desirable characteristics such as reducing damage and contamination without incurring cost as taught by Enomoto in col. 1 lines 38-42 and col. 4 lines 28-37.

Regarding claim 40, as discussed in the above claims 1-4, and 12, the combination of Chang and Enomoto disclose all the limitations of claim 40.

5. Claims 6, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6004829 to Chang et al. and US 5506159 to Enomoto as applied to claims 1 and 9 above and further in view of US 6406959 to Prall et al (of record).

Regarding claims 6, 13, Chang does not expressly disclose the semiconductor IC device wherein a SOI substrate is employed as substrate.

However, Prall reference discloses a flash memory device wherein the substrate 11 can be either silicon or SOI, column 4 line 15. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to replace the silicon substrate of Chang with either Si or SOI substrate teaching of Prall, because such substrate substitution would have been considered a mere substitution of art-recognized equivalent values.

6. Claims 8 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6004829 to Chang et al and US 5506159 to Enomoto as applied to claims 1 and 9 above and further in view of Applicant Admitted Prior Art (APA)

Regarding to claims 8 and 15, Chang does not discloses the tunnel insulating film is a nitride oxide film.

However, APA discloses the IC device having the tunnel oxide 12, spec. page 2 or nitride, page 4. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to use the tunnel insulating material teaching of APA in the Chang's device, because such material substitution would have been considered a mere substitution of art-recognized equivalent values.

7. Claims 1 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6417044 to Ono in view of US 6294430 to Fastow et al.

Regarding claims 1 and 9, Ono discloses a semiconductor integrated circuit device in fig. 3 comprising: a substrate (101), a nonvolatile memory device formed in a memory cell region (with gate 111 and 107) of said substrate (101), the nonvolatile memory device comprising: a first active region (104) covered with a tunnel insulating film (106), a second active region (102) formed next to the first active region (104) and covered with an insulating film (106), a control gate (111) formed of an embedded diffusion region formed in the first active region; a first gate electrode (107) extending on the tunnel insulating film (106) in the first active region and forming a bridge between the first and second active regions to be capacitive-coupled via the insulating film (109) to the embedded diffusion region in the first active region, the first gate electrode (107) having sidewall faces thereof covered with a protection insulating film (112) formed of a oxide film; and a diffusion region (N-) formed on each of sides of the first gate electrode (107) in the first active region; and a semiconductor device formed in a device region (NWell) of substrate (101), the semiconductor device comprising a gate insulating film (106) covering substrate (101) and a second gate electrode (107) formed on the gate insulating film (106), fig. 3, and the gate insulating film (106) is interposed between said substrate (101) and the second gate electrode (107) to have a uniform thickness at the region under the entire gate electrode (107), fig. 3; wherein the protective insulating film (112) covers a top surface of the first gate electrode; and sidewalls are formed over the first gate (107), said the sidewalls covering the entire side surface of the first gate electrode (107) and the first gate electrode (107) has a substantially uniform width, fig. 3.

But, Ono does not disclose wherein the bird's beak structure is formed at an interface of the tunnel insulating film and the floating gate electrode the bird's beak structure penetrating into the floating gate electrode along the interface from the sidewall faces of the floating gate electrode and sidewalls are formed over the protection insulating film, said side walls covering the entire surface of the multilayer gate electrode structure.

However, Fastow discloses a semiconductor device in fig. 3G comprising a first active region n and n+ (double diffused regions), fig. 1 and fig. 3G, a bird's beak (334), a tunnel oxide, a floating gate 308, a ONO dielectric 310, a control gate 312 and a protective insulating film 314 continuously covers sidewall faces and a top surface of the multilayer gate electrode structure and wherein the protective insulating film covers the multilayer gate electrode uniformly; and sidewall are 332 are formed over the protecting insulating film 314, said sidewalls covering the entire side surface of the first gate electrode, fig. 3G . At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the double diffused regions and protective insulating film 314 and sidewalls 332 teaching of Fastow with Ono's device, because it would have created an EEPROM device reducing the number of oxides traps in the bird's beak region of the tunnel oxide thus improving the reliability of the floating gate memory device as taught by Fastow in col. 1 lines 10-15.

Response to Arguments

8. Applicant's arguments with respect to claims 1-4, 6-10, 12-15 and 40 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

25 Oct. 2007

/Thao X Le/
Primary Examiner, Art Unit 2814